

Model Name:GA-970A-UD3P

Component value change history

Version: 1.02

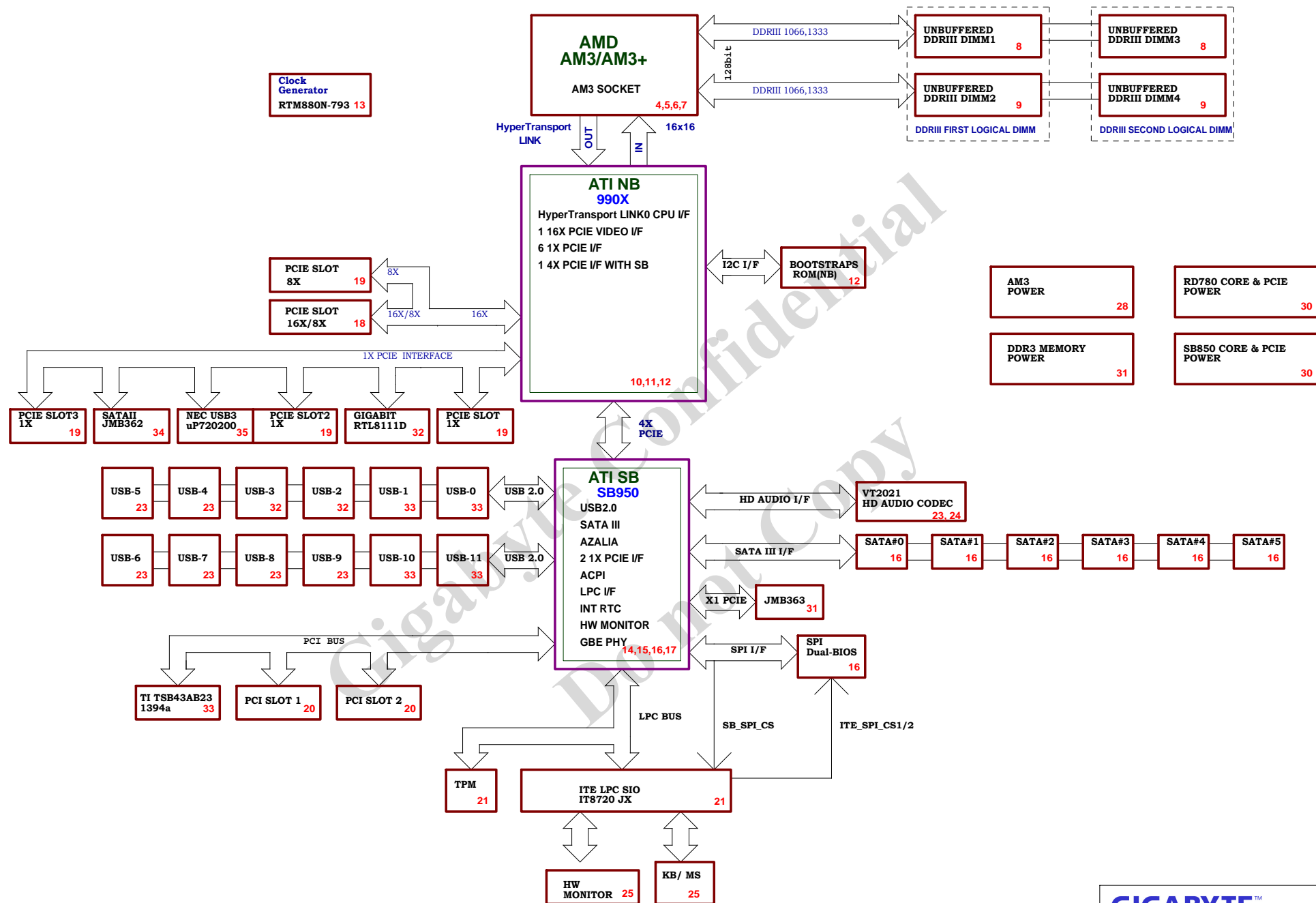
4 Layer, 4mil 50ohm +/- 15% L

P-Code: U98094-0

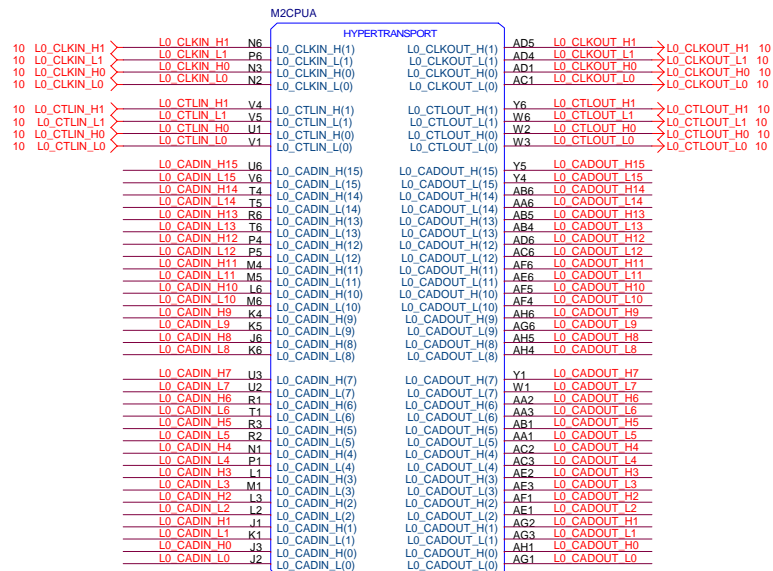
Circuit or PCB layout change for next version

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Title			
BOM & PCB HISTORY			
Size	Document Number	Rev	
Custom	GA-970A-UD3P	1.02	
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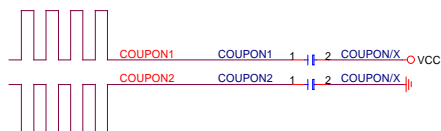
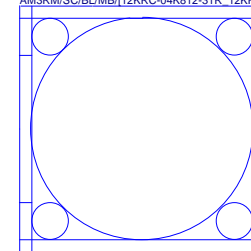
L0_CADIN_L[0..15] < L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 10



CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-04R]

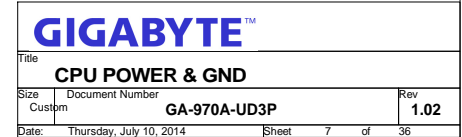
CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

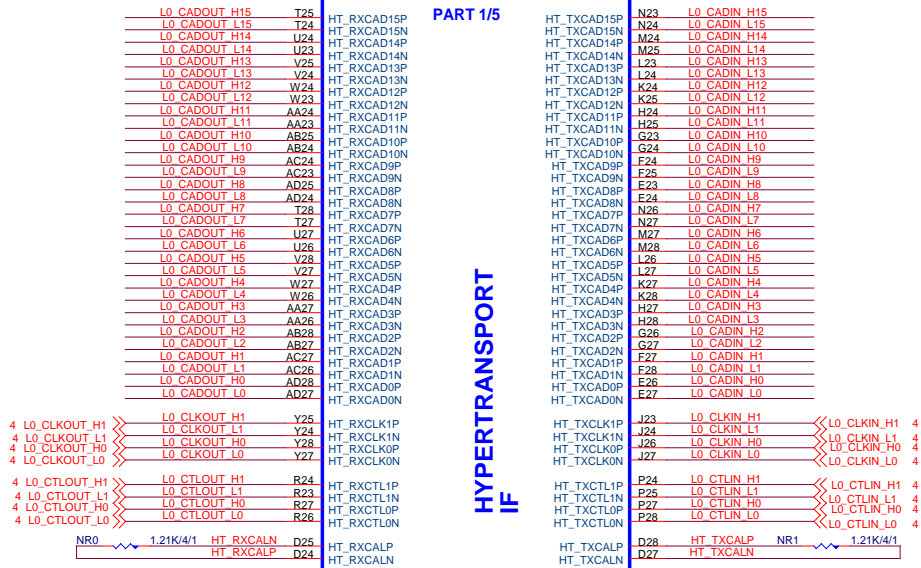
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Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custpm	GA-970A-UD3P	1.02	
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U3A

PART 1/5

HYPERTRANSPORT
IF

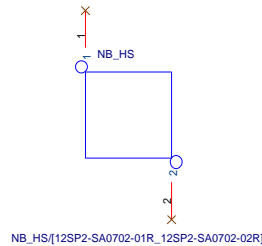
RX980/BGA692

L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 4

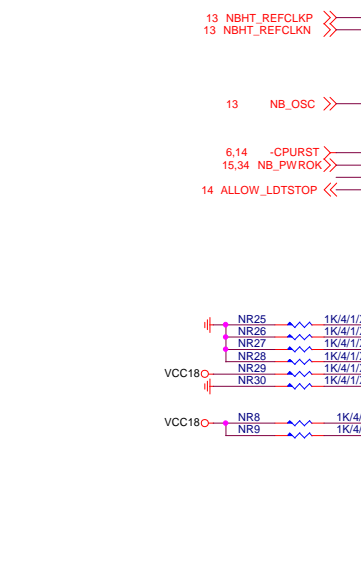
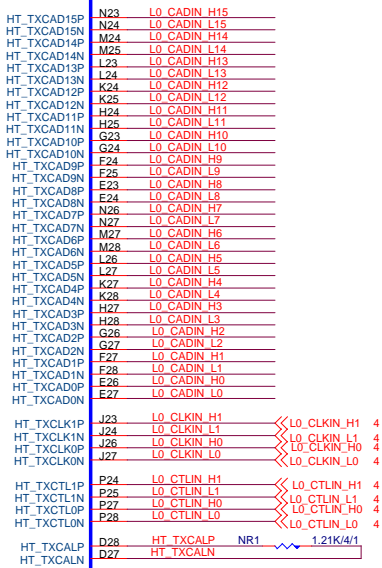
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 4

L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 4

L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 4



NB_HS[12SP2-SA0702-01R_12SP2-SA0702-02R]



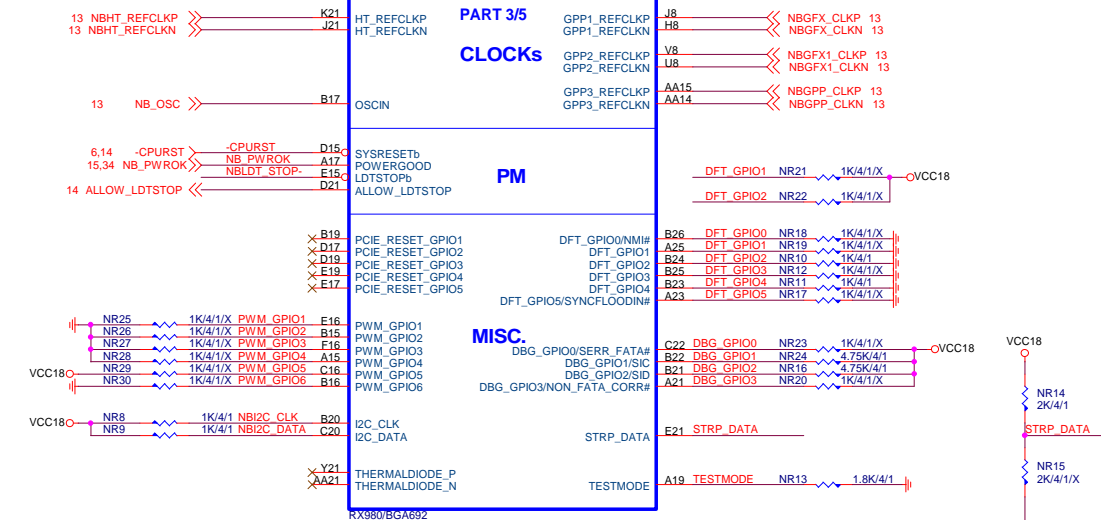
U3C

PART 3/5

CLOCKS

PM

MISC.



DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO4[2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title RS780 HT-LINK I/F

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U3B

PART 2/5

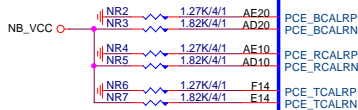
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EXP A RXN15	N5	GPP1_RX15N	GPP1_TX15N	M2	EXP A TXN15
EXP A RXP14	M5	GPP1_RX14P	GPP1_TX14P	M1	EXP A TXN14
EXP A RXN14	M4	GPP1_RX14N	GPP1_TX14N	L3	EXP A TXP13
EXP A RXP13	L6	GPP1_RX13P	GPP1_TX13P	L2	EXP A TXN13
EXP A RXN13	L5	GPP1_RX13N	GPP1_TX13N	K2	EXP A TXP12
EXP A RXP12	K5	GPP1_RX12P	GPP1_TX12P	K1	EXP A TXN12
EXP A RXN12	K4	GPP1_RX12N	GPP1_TX12N	J3	EXP A TXP11
EXP A RXP11	J6	GPP1_RX11P	GPP1_TX11P	J2	EXP A TXN11
EXP A RXN11	J5	GPP1_RX11N	GPP1_TX11N	H2	EXP A TXP10
EXP A RXP10	H5	GPP1_RX10P	GPP1_TX10P	H1	EXP A TXN10
EXP A RXN10	H4	GPP1_RX10N	GPP1_TX10N	G3	EXP A TXP9
EXP A RXP9	G6	GPP1_RX9P	GPP1_TX9P	G2	EXP A TXN9
EXP A RXN9	G5	GPP1_RX9N	GPP1_TX9N	F2	EXP A TXP8
EXP A RXP8	F5	GPP1_RX8P	GPP1_TX8P	F1	EXP A TXN8
EXP A RXN8	F4	GPP1_RX8N	GPP1_TX8N	E3	EXP A TXP7
EXP A RXP7	D2	GPP1_RX7P	GPP1_TX7P	E2	EXP A TXN7
EXP A RXN7	D1	GPP1_RX7N	GPP1_TX7N	A4	EXP A TXP6
EXP A RXP6	B5	GPP1_RX6P	GPP1_TX6P	B4	EXP A TXN6
EXP A RXN6	C6	GPP1_RX6N	GPP1_TX6N	A6	EXP A TXP5
EXP A RXP5	D6	GPP1_RX5P	GPP1_TX5P	B6	EXP A TXN5
EXP A RXN5	E6	GPP1_RX5N	GPP1_TX5N	B7	EXP A TXP4
EXP A RXP4	E7	GPP1_RX4P	GPP1_TX4P	C7	EXP A TXN4
EXP A RXN4	F7	GPP1_RX4N	GPP1_TX4N	A8	EXP A TXP3
EXP A RXP3	D8	GPP1_RX3P	GPP1_TX3P	B8	EXP A TXN3
EXP A RXN3	E8	GPP1_RX3N	GPP1_TX3N	B9	EXP A TXP2
EXP A RXP2	E9	GPP1_RX2P	GPP1_TX2P	C9	EXP A TXN2
EXP A RXN2	F9	GPP1_RX2N	GPP1_TX2N	A10	EXP A TXP1
EXP A RXP1	D10	GPP1_RX1P	GPP1_TX1P	B10	EXP A TXN1
EXP A RXN1	E10	GPP1_RX1N	GPP1_TX1N	B11	EXP A TXP0
EXP A RXP0	E11	GPP1_RX0P	GPP1_TX0P	C11	EXP A TXN0
EXP A RXN0	F11	GPP1_RX0N	GPP1_TX0N		

AC9	GPP2_RX15P	GPP2_TX15P	AF9
AD9	GPP2_RX15N	GPP2_TX15N	AG9
AE8	GPP2_RX14P	GPP2_TX14P	AG8
AC7	GPP2_RX14N	GPP2_TX14N	AH8
AD7	GPP2_RX13P	GPP2_TX13P	AF7
AD6	GPP2_RX13N	GPP2_TX13N	AG7
AE6	GPP2_RX12P	GPP2_TX12P	AG6
AE5	GPP2_RX12N	GPP2_TX12N	AH6
AG5	GPP2_RX11P	GPP2_TX11P	AG4
AF2	GPP2_RX11N	GPP2_TX11N	AH4
AD2	GPP2_RX10P	GPP2_TX10P	AE3
AD1	GPP2_RX10N	GPP2_TX10N	AE2
AB5	GPP2_RX9P	GPP2_TX9P	AC3
AB4	GPP2_RX8P	GPP2_TX8P	AC2
AA6	GPP2_RX8N	GPP2_TX8N	AB2
AA5	GPP2_RX7P	GPP2_TX7P	AB1
Y5	GPP2_RX7N	GPP2_TX7N	AA3
V4	GPP2_RX6P	GPP2_TX6P	AA2
W6	GPP2_RX6N	GPP2_TX6N	Y2
W5	GPP2_RX5P	GPP2_TX5P	V1
V5	GPP2_RX5N	GPP2_TX5N	W3
V4	GPP2_RX4P	GPP2_TX4P	W2
U6	GPP2_RX4N	GPP2_TX4N	V2
U5	GPP2_RX3P	GPP2_TX3P	V1
T5	GPP2_RX3N	GPP2_TX3N	U2
T4	GPP2_RX2P	GPP2_TX2P	T2
R6	GPP2_RX2N	GPP2_TX2N	T1
R5	GPP2_RX1P	GPP2_TX1P	R3
P5	GPP2_RX1N	GPP2_TX1N	R2
P4	GPP2_RX0P	GPP2_TX0P	P2
	GPP2_RX0N	GPP2_TX0N	P1

AD11	GPP3_RX9P	GPP3_TX9P	AH10
AC11	GPP3_RX9N	GPP3_TX9N	AG10
AE12	GPP3_RX8P	GPP3_TX8P	AG11
AD13	GPP3_RX8N	GPP3_TX8N	AE11
AC13	GPP3_RX7P	GPP3_TX7P	AH12
AD14	GPP3_RX7N	GPP3_TX7N	AG12
AE14	GPP3_RX6P	GPP3_TX6P	AE13
AD15	GPP3_RX6N	GPP3_TX6N	AH14
AC15	GPP3_RX5P	GPP3_TX5P	AG14
AE16	GPP3_RX5N	GPP3_TX5N	AG15
AD16	GPP3_RX4P	GPP3_TX4P	AE15
AD17	GPP3_RX4N	GPP3_TX4N	AH16
AC17	GPP3_RX3P	GPP3_TX3P	AG16
AE18	GPP3_RX3N	GPP3_TX3N	AG17
AD18	GPP3_RX2P	GPP3_TX2P	AE17
AD19	GPP3_RX2N	GPP3_TX2N	AH18
AC19	GPP3_RX1P	GPP3_TX1P	AG18
AC19	GPP3_RX1N	GPP3_TX1N	AG19
AH20	GPP3_RX0P	GPP3_TX0P	AF19
AG20	GPP3_RX0N	GPP3_TX0N	

AC21	SB_RX3P	SB_TX3P	AG22
AD21	SB_RX3N	SB_TX3N	AH22
AE22	SB_RX2P	SB_TX2P	AG21
AF25	SB_RX2N	SB_TX2N	AG21
AG25	SB_RX1P	SB_TX1P	AF23
AG26	SB_RX1N	SB_TX1N	AG23
AH26	SB_RX0P	SB_TX0P	AG24
	SB_RX0N	SB_TX0N	AH24

RX980/BGA692



PCI E slot TX need CAP close to slot side

PLACE THESE CAP CLOSE TO NB.

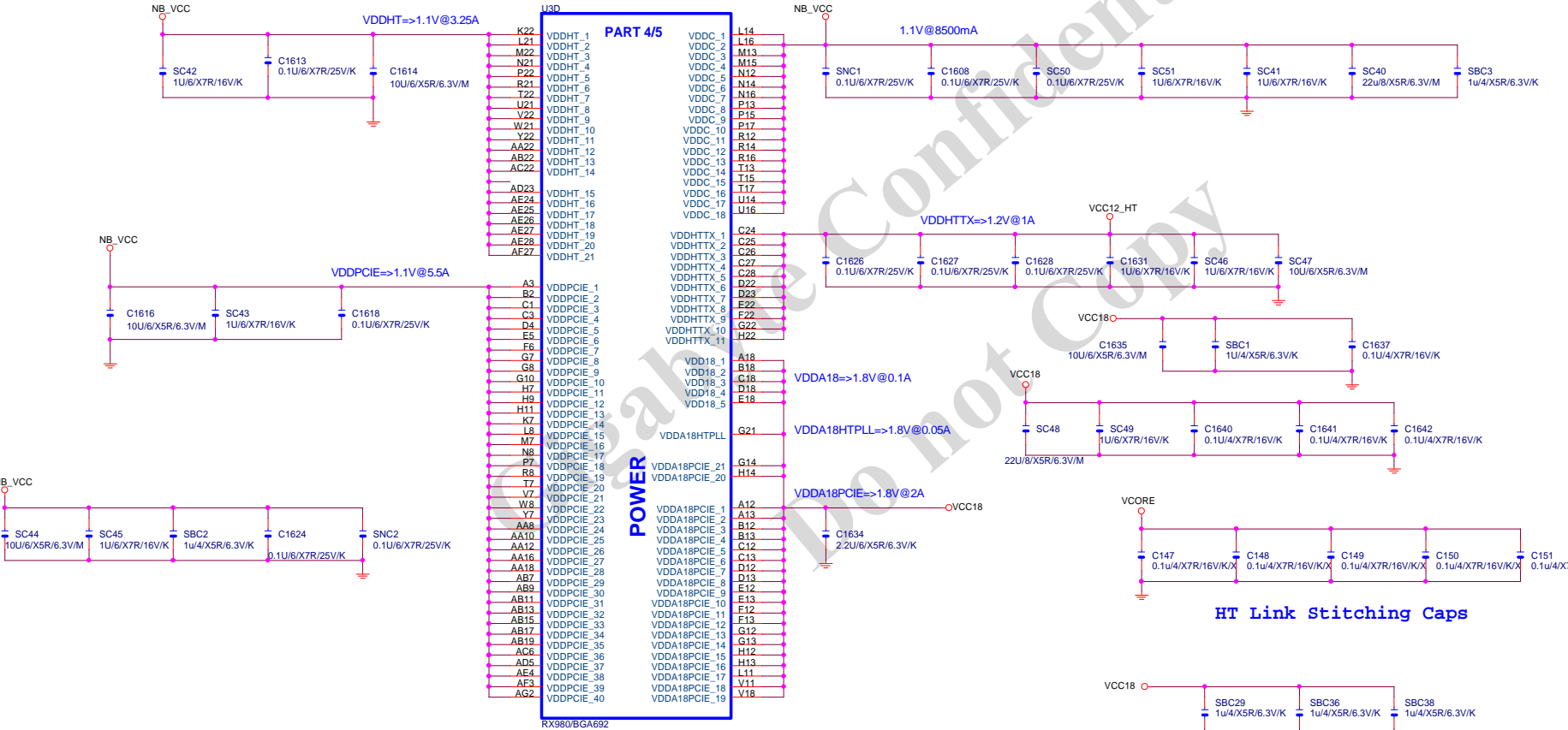
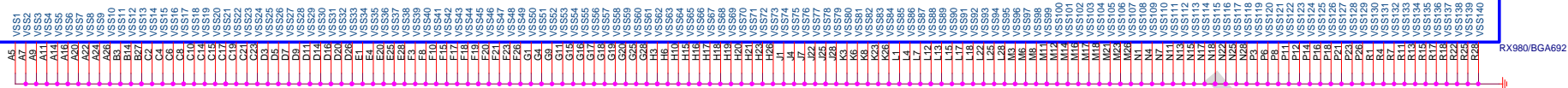
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Title
RS780 PCIe I/F ,SwitchSize
Document Number
Custpm
GA-970A-UD3PRev
1.02

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PART 5/5

GROUND



NB CLOCK INPUT TABLE

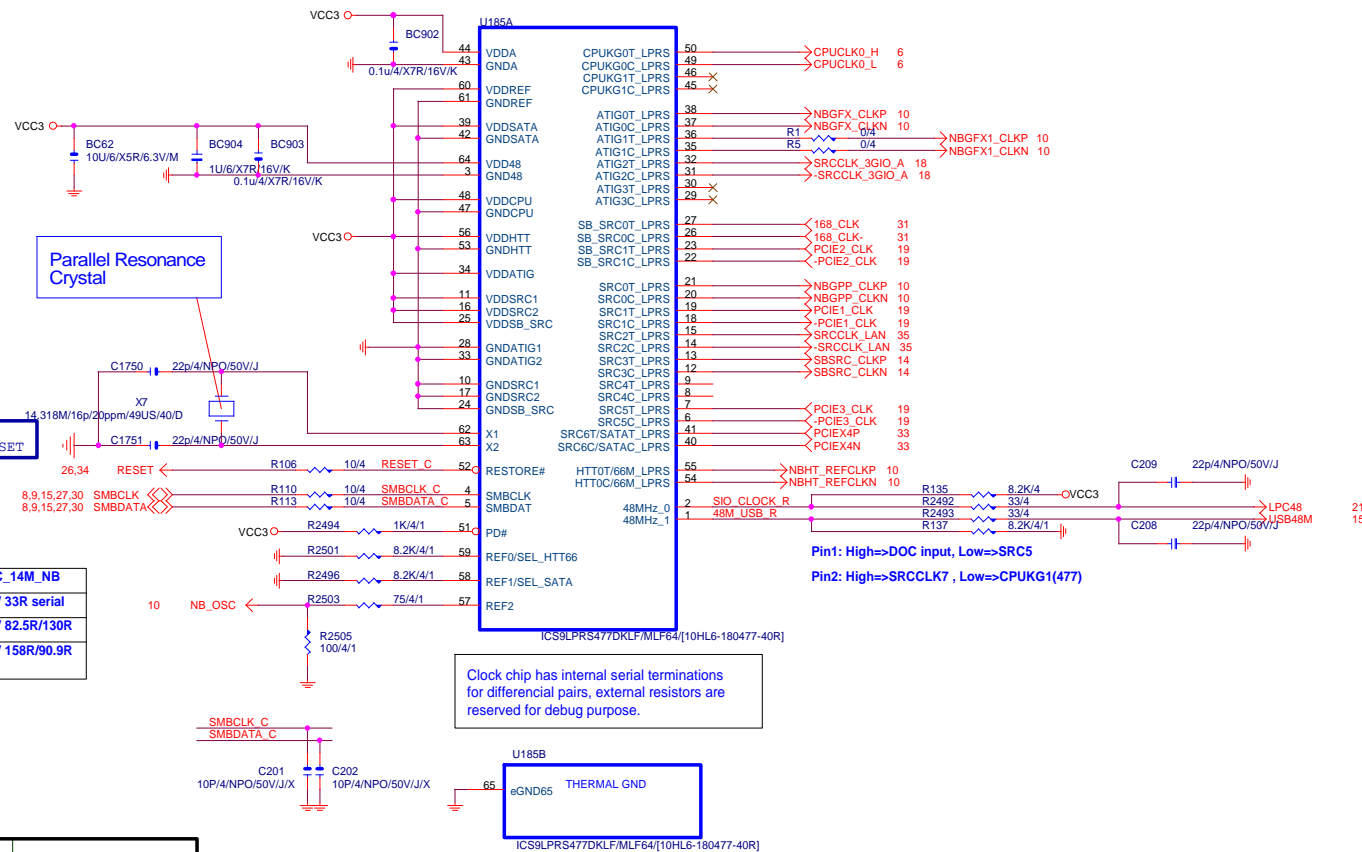
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
 R851 less than 100 mils away from R800/801
 route CPU clock as 100ohm differential pair



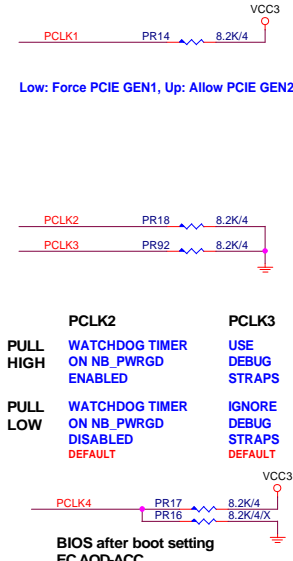
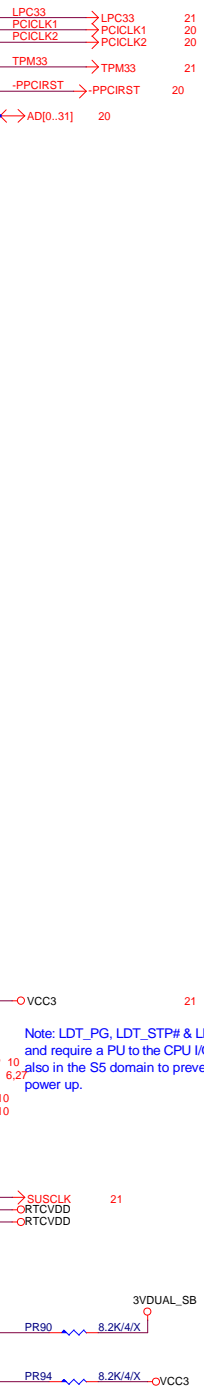
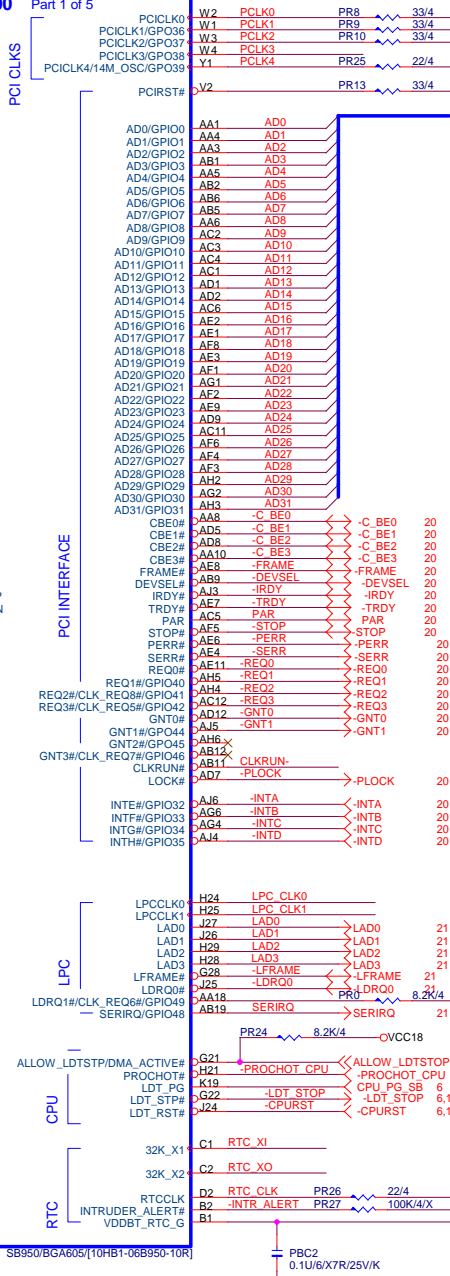
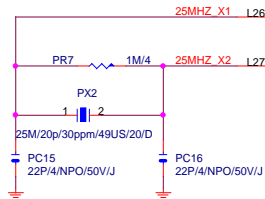
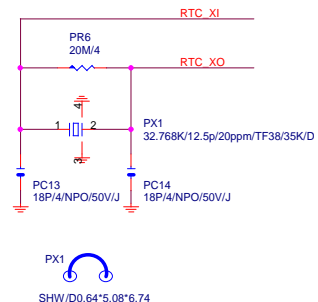
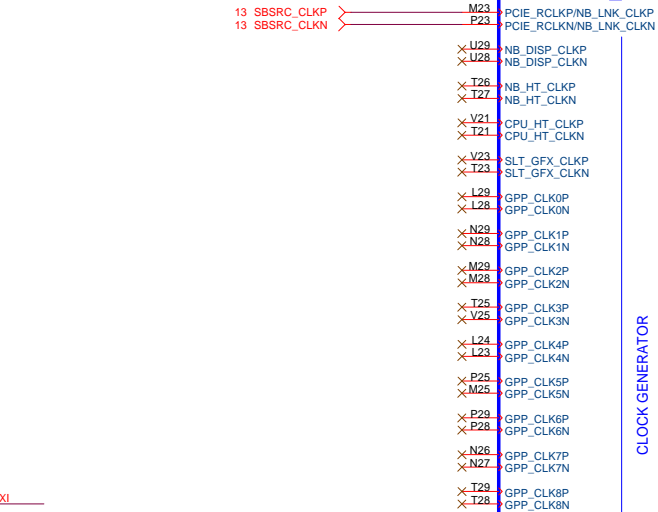
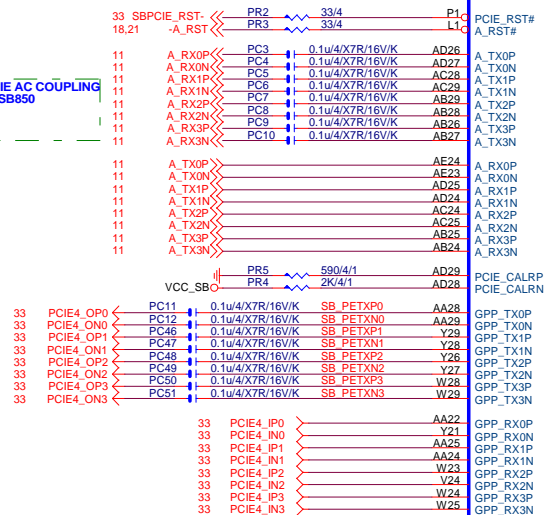
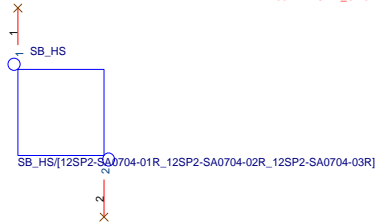
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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



PULL HIGH WATCHDOG TIMER ON NB_PWRGD ENABLED

PULL LOW WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT

PULL HIGH IMC ENABLED AOD Extreme

PULL LOW IMC DISABLED DEFAULT

USE DEBUG STRAPS

IGNORE DEBUG STRAPS

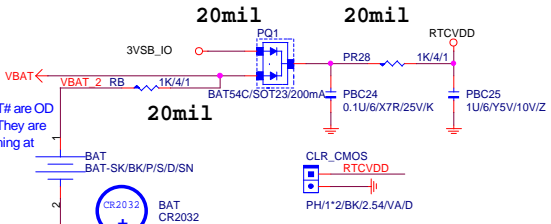
BIOS after boot setting EC AOD-ACC

LPC_CLK0 Rev.A12

LPC_CLK1

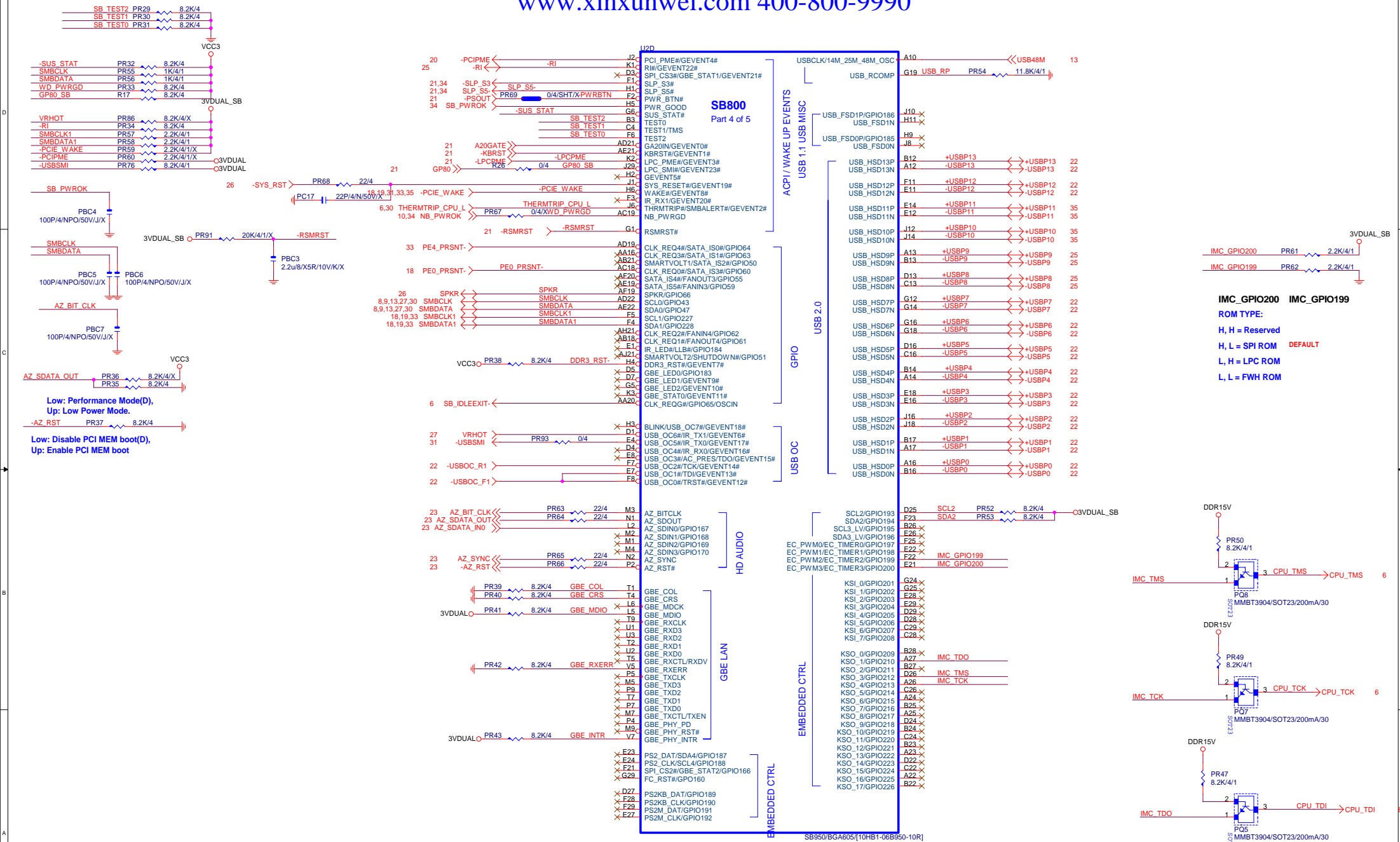
CLKGEN ENABLED

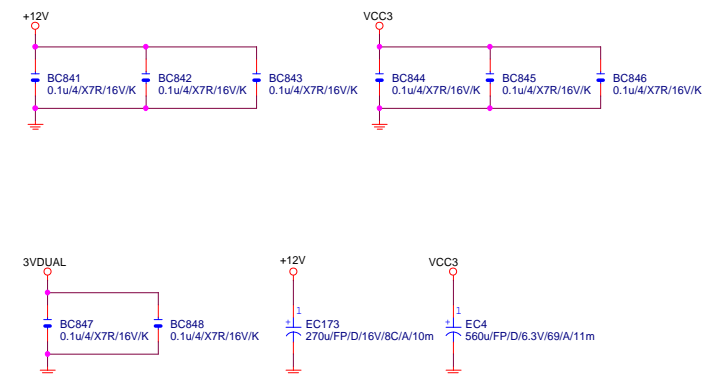
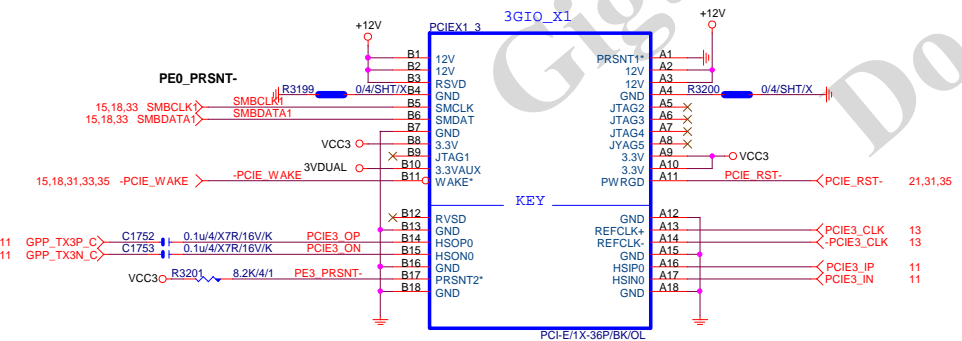
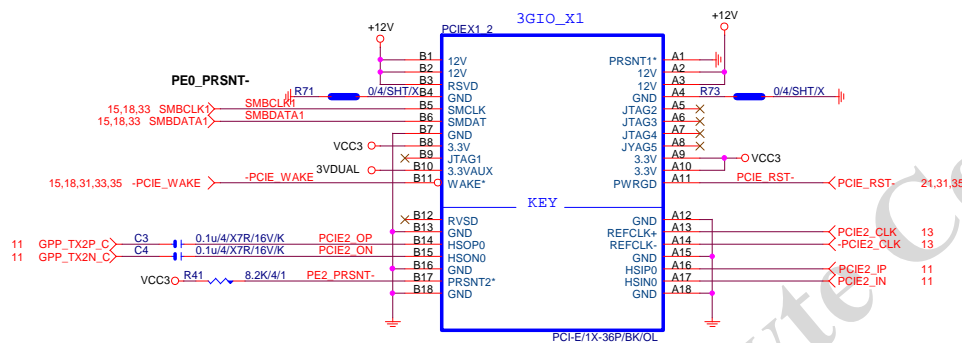
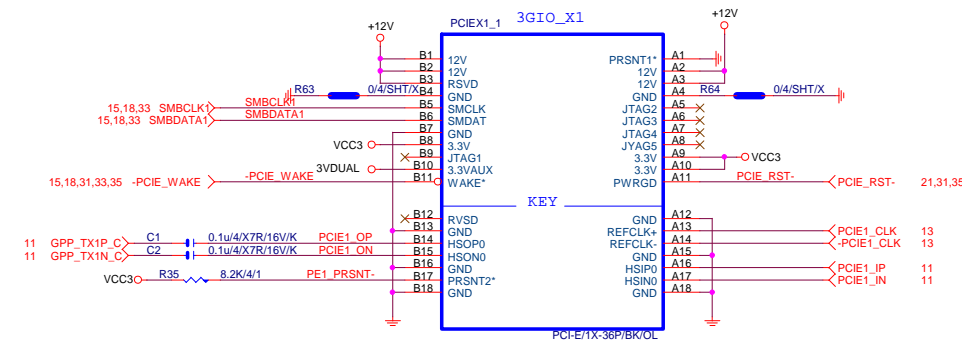
CLKGEN DISABLED



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

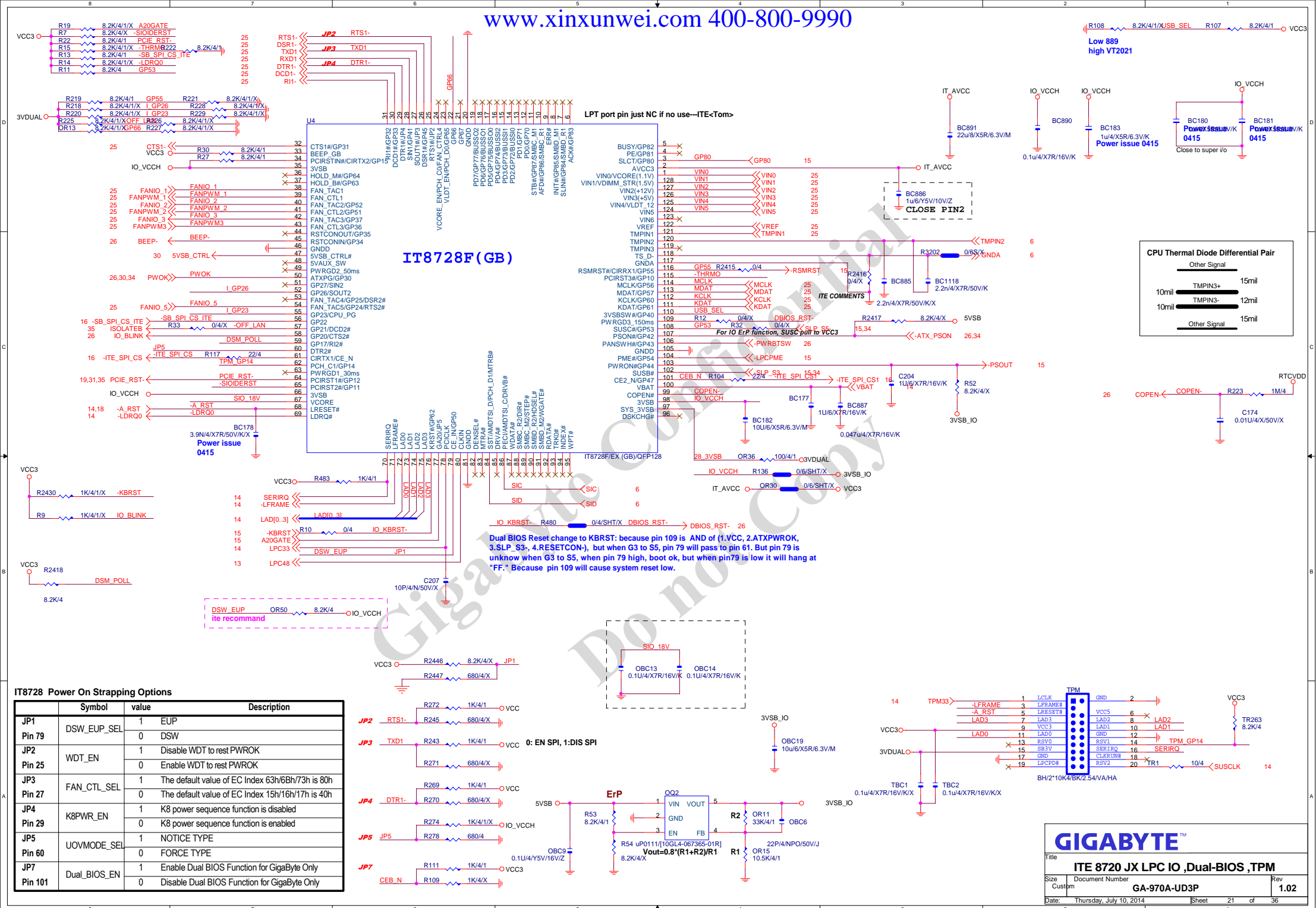




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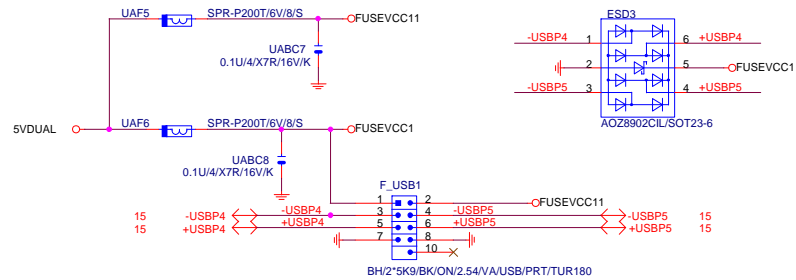
Title
PCI_E x8 ,PCI_E x1 SLOT 1,2

Size	Document Number	Rev
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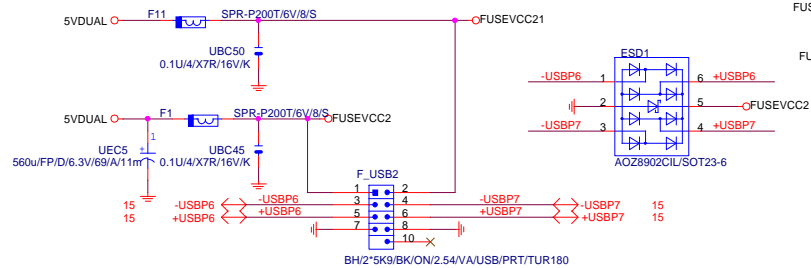


IT8728 Power On Strapping Options			
	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 79		0	DSW
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin 25		0	Enable WDT to rest PWROK
JP3	FAN_CTL_SEL	1	The default value of EC Index 63h/6Bh/73h is 80h
Pin 27		0	The default value of EC Index 15h/16h/17h is 40h
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 29		0	K8 power sequence function is enabled
JP5	UOVMODE_SEL	1	NOTICE TYPE
Pin 60		0	FORCE TYPE
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 101		0	Disable Dual BIOS Function for GigaByte Only

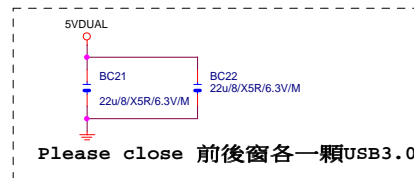
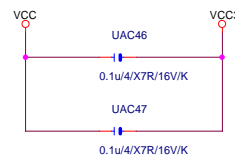
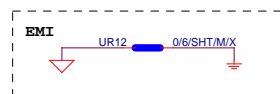
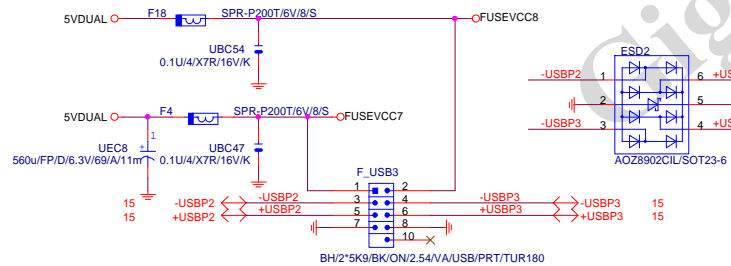
FRONT SIDE USB1



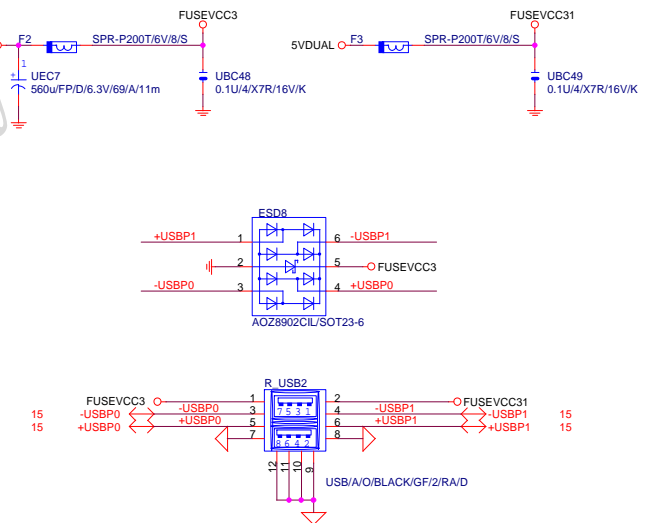
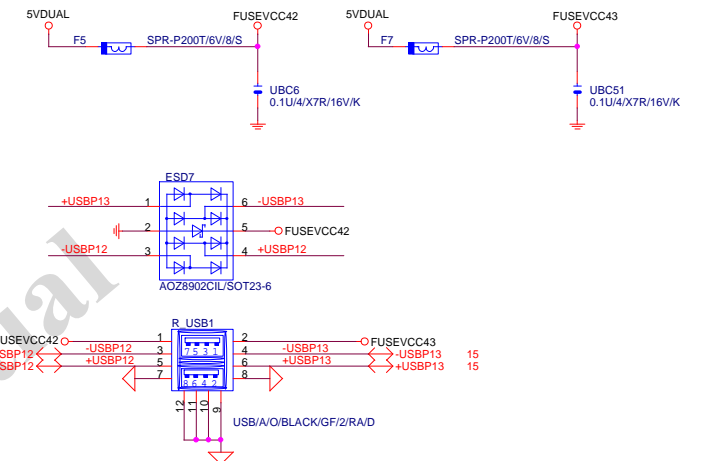
FRONT SIDE USB2



FRONT SIDE USB3



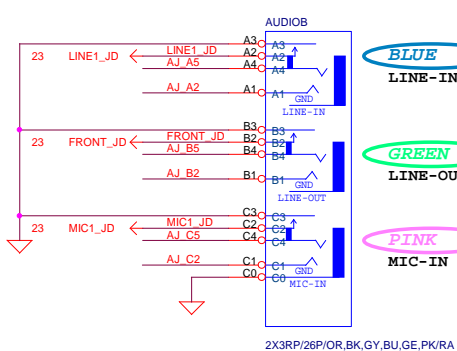
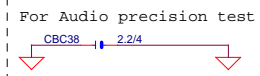
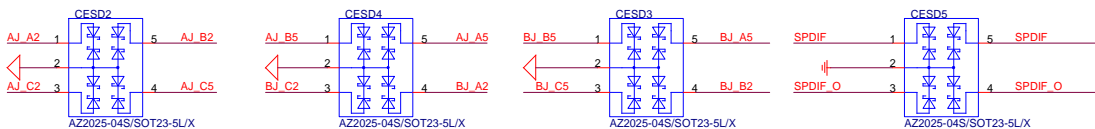
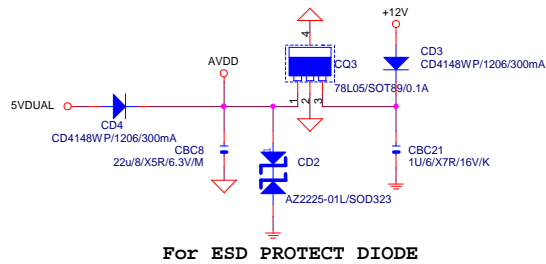
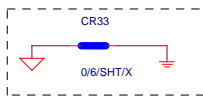
REAR USB



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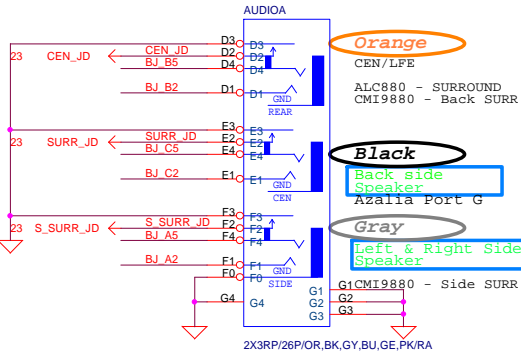
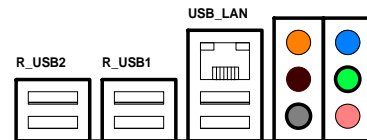
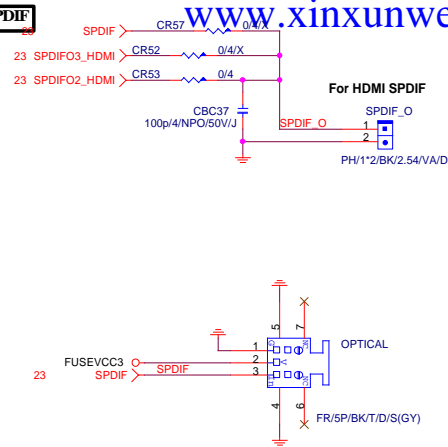
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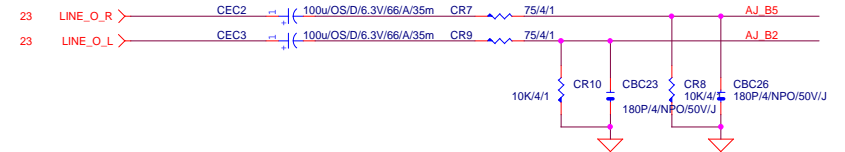
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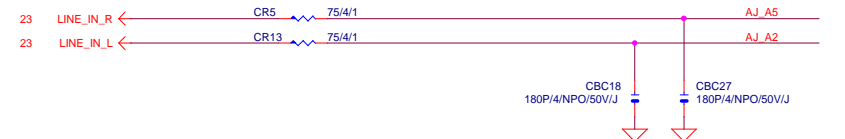


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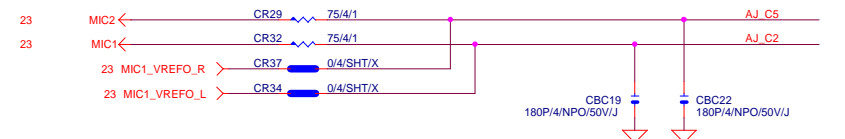
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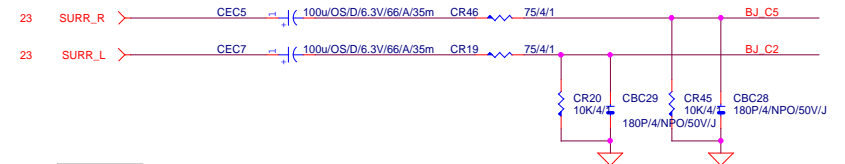
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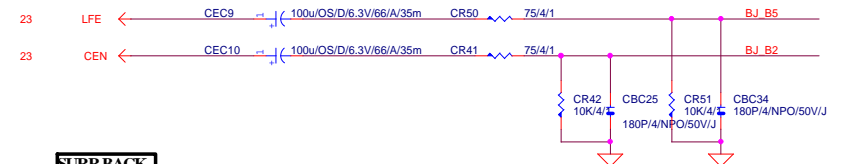
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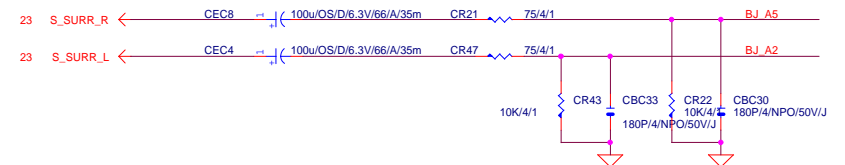
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CEN/LFE



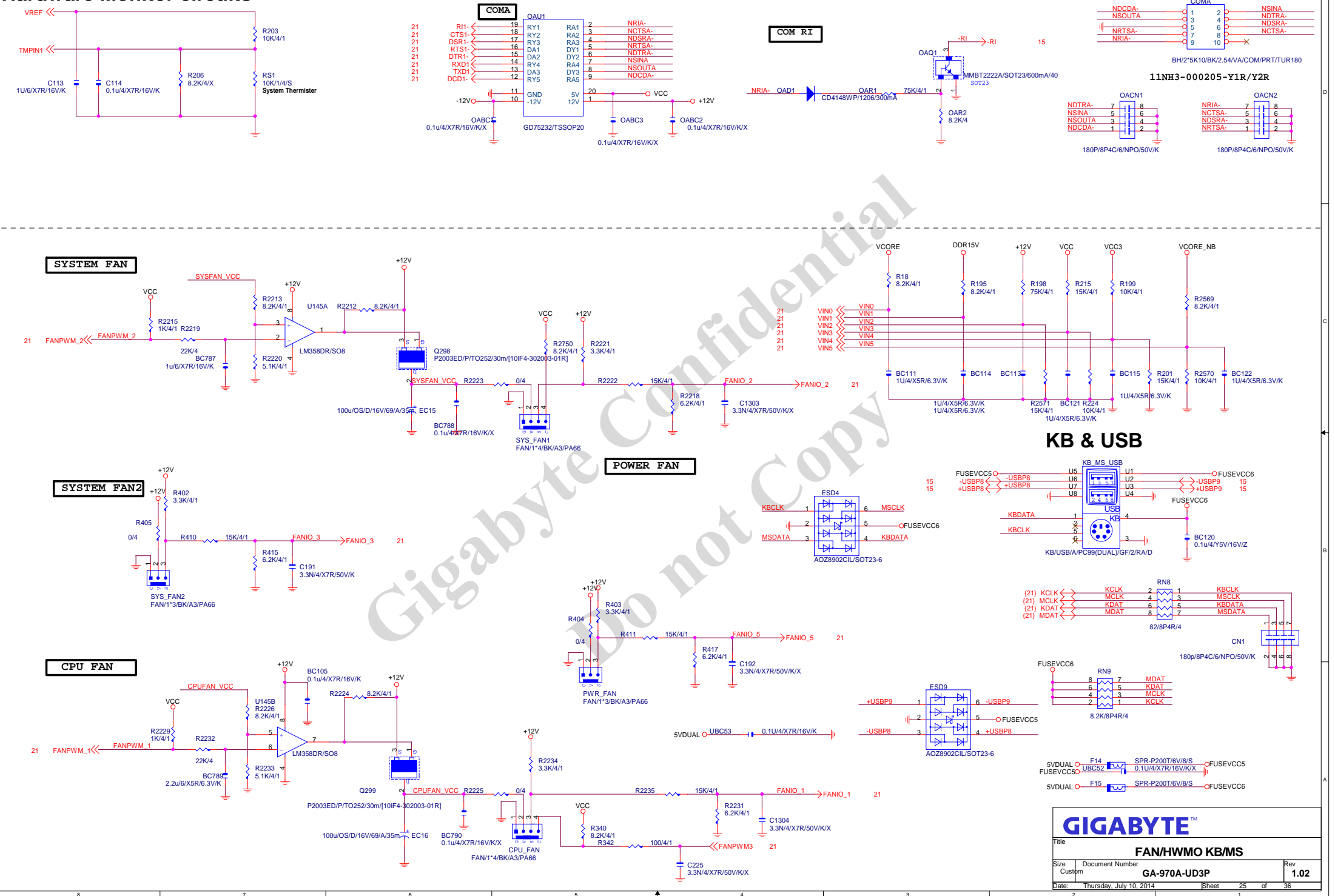
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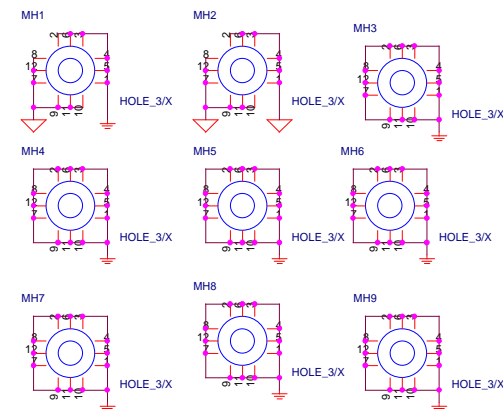
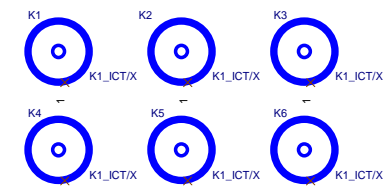
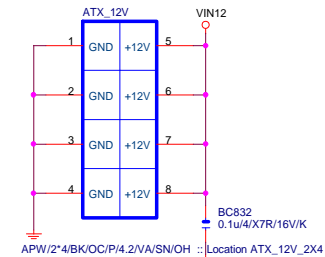
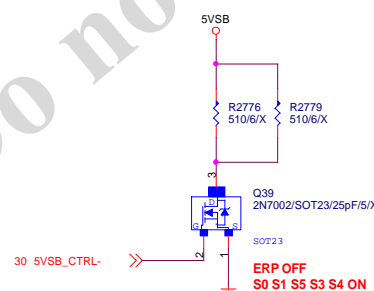
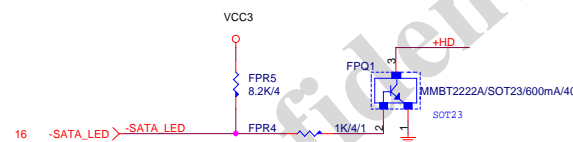
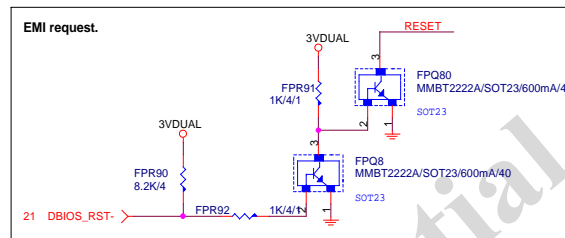
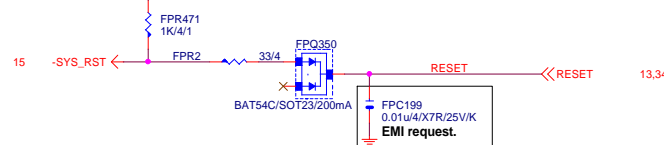
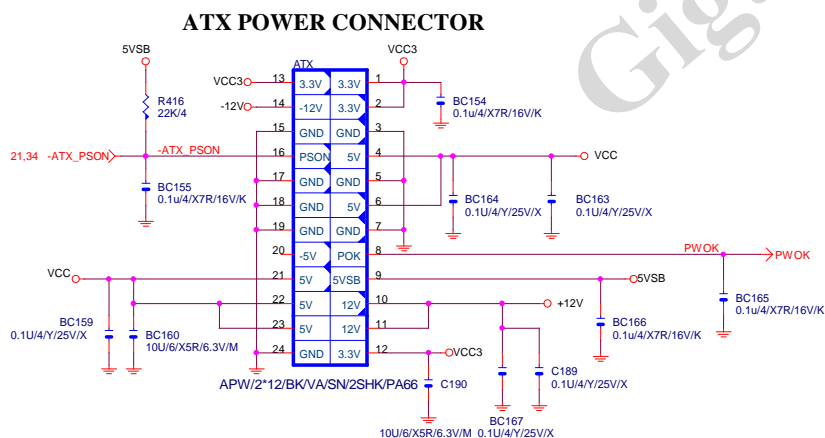
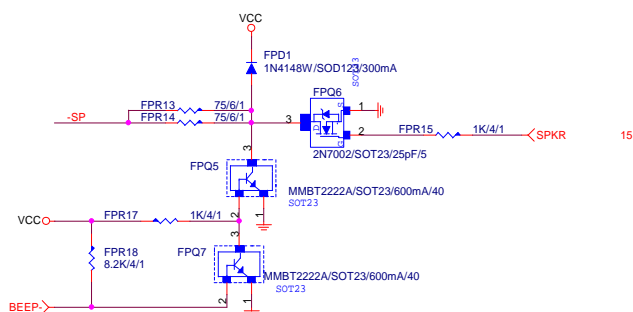
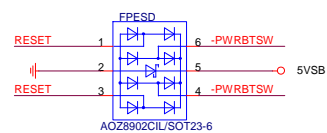
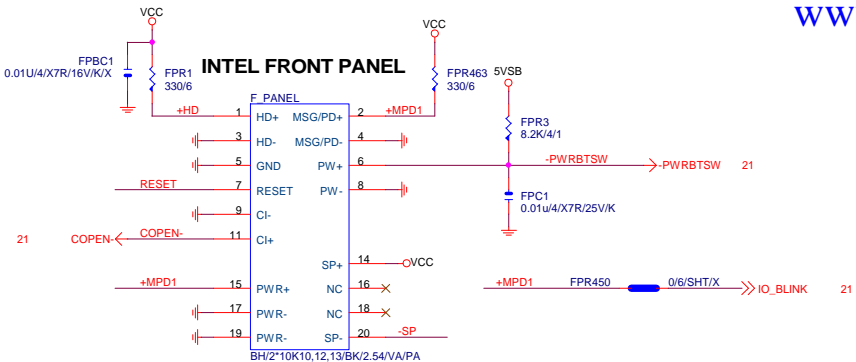


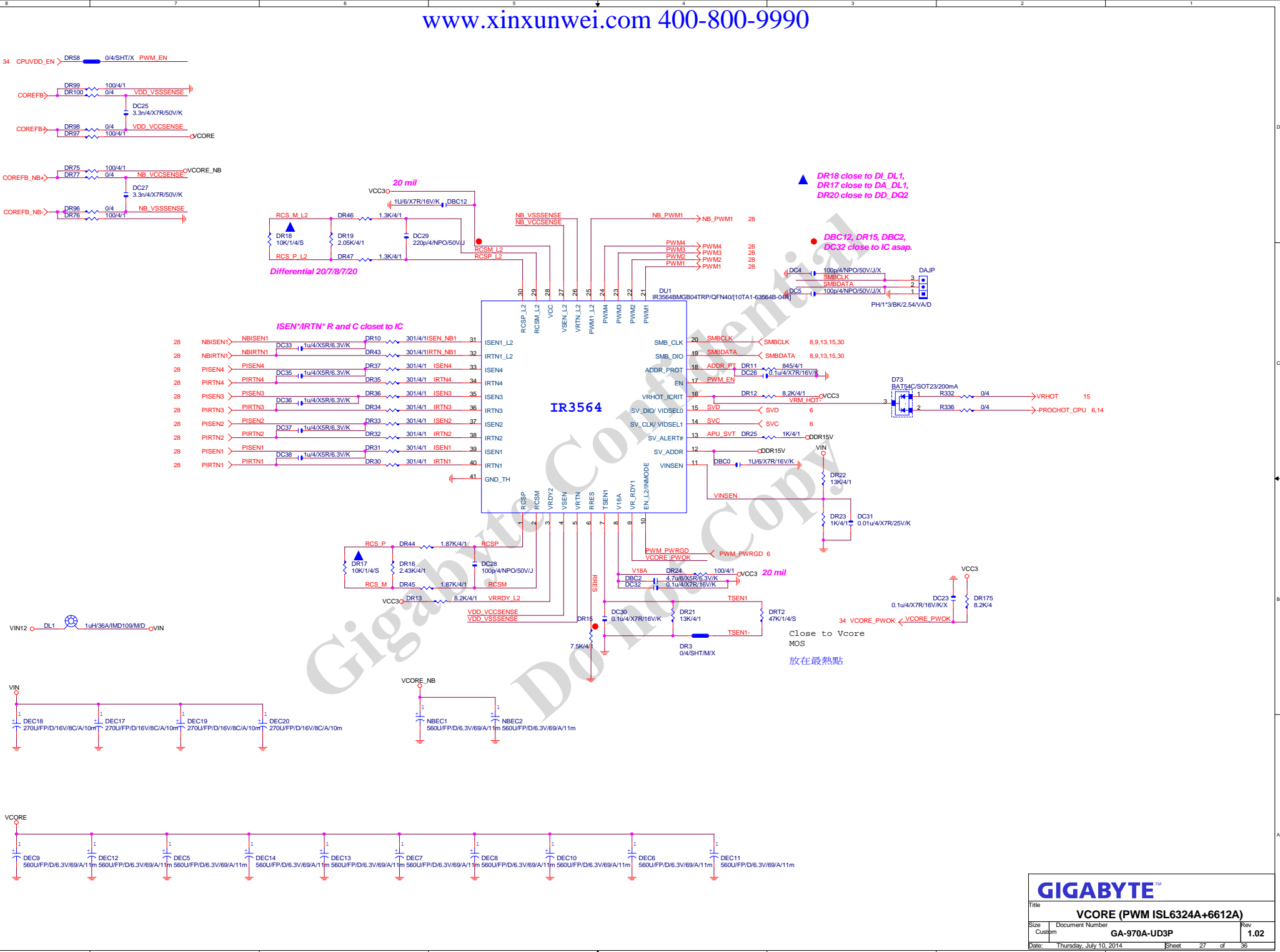
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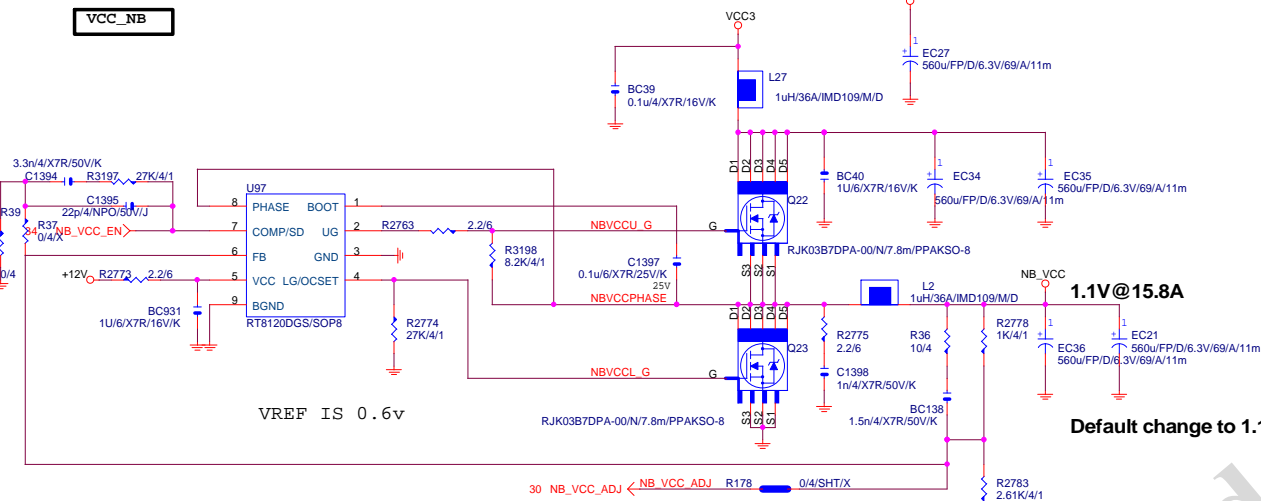
Hardware Monitor circuits



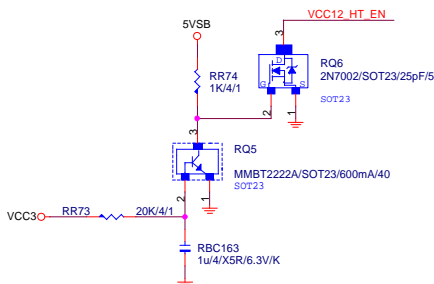
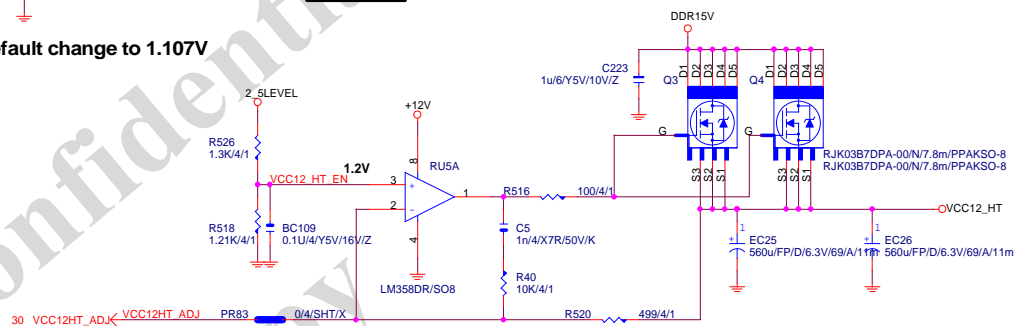




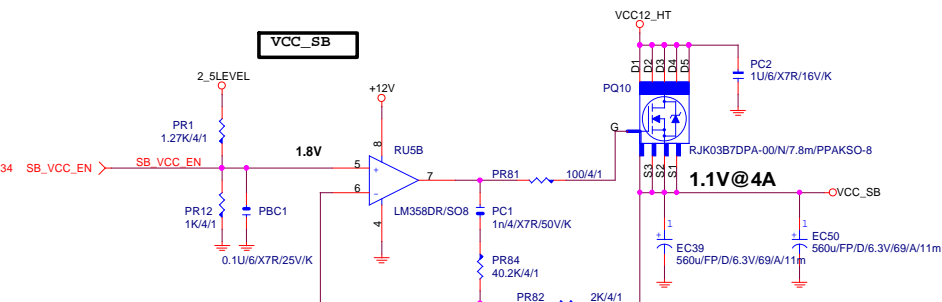
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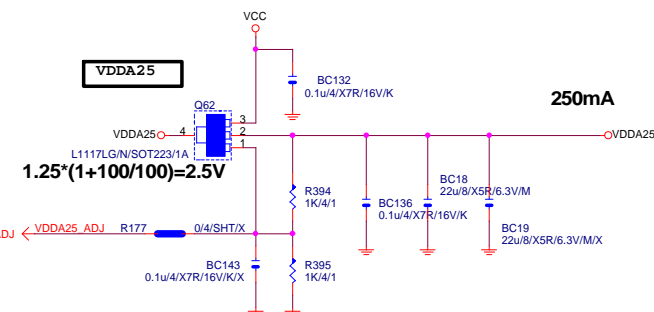
VCC12_HT



VCC_SB



VDDA25



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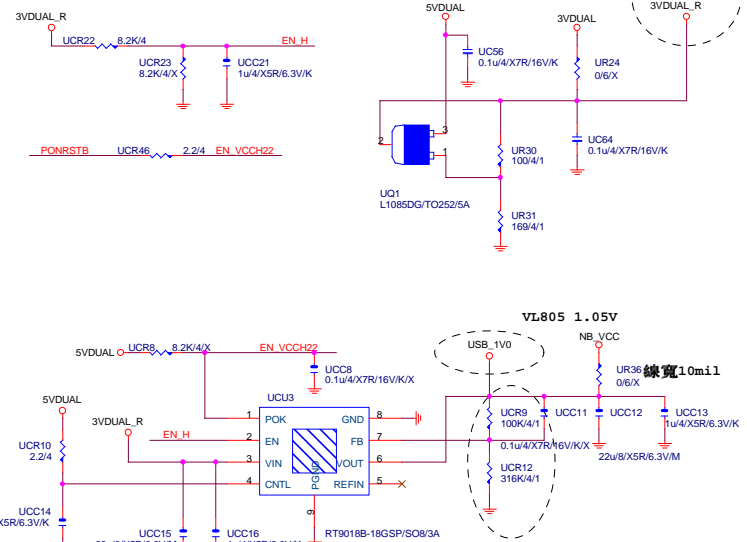
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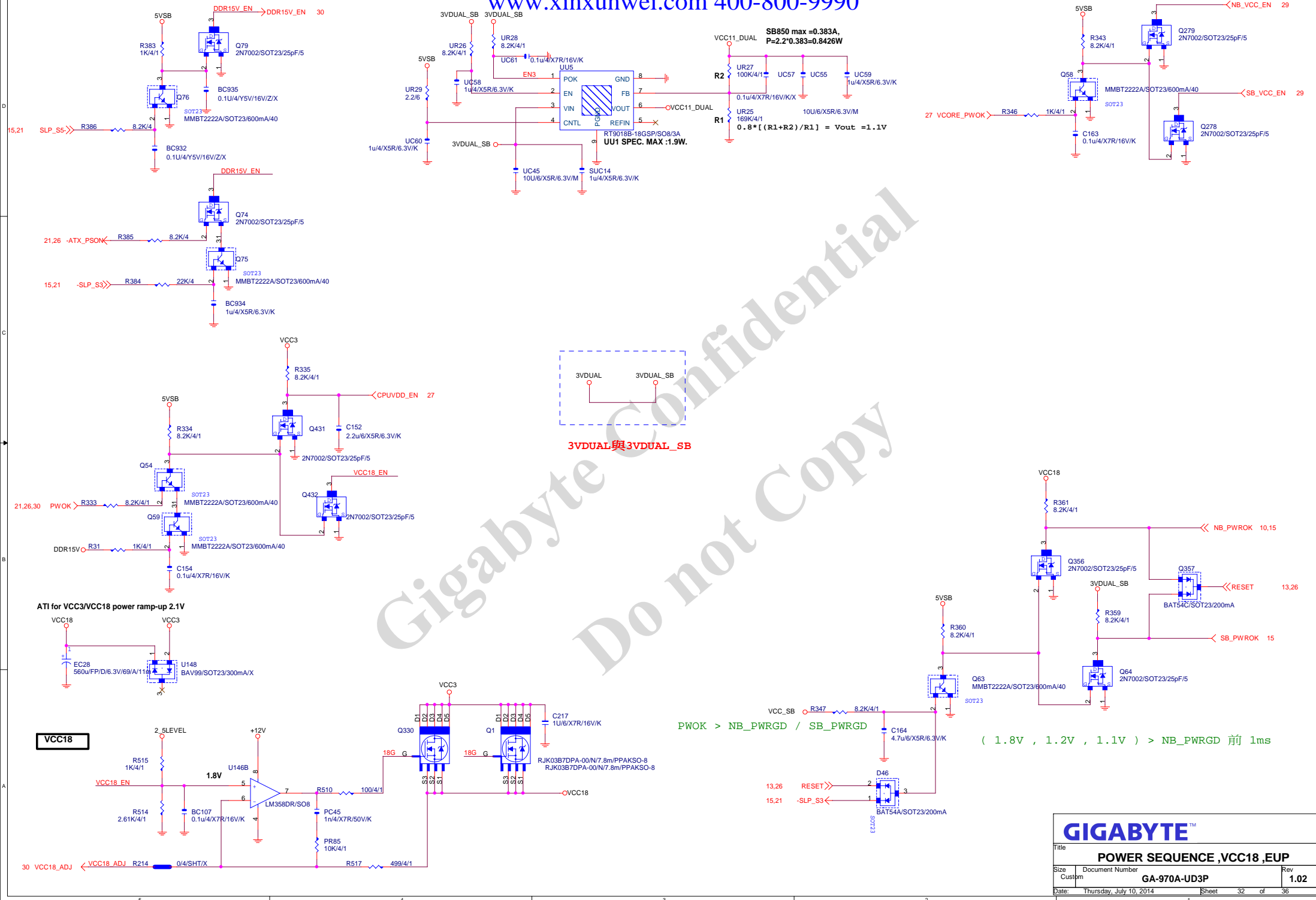
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FRONT SIDE USB3

REAR SIDE USB3

